2811

PATENT APPLICATION
Do. No. 9898-188

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Mun-Mo JEONG

Serial No. 10/003,386 Examiner: Gebremariam, Samuel A

Confirmation No. 5232

Filed: October 30, 2001 Group Art Unit: 2811

For: SEMICONDUCTOR DEVICE WITH CONTACTS HAVING UNIFORM CONTACT RESISTANCE AND METHOD FOR MANUFACTURIG THE SAME

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents,
Washington, D.C. 20231

Responsive to the Office Action dated August 14, 2002, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	25 ~~18~~	20	0	x $18 =	~~$0~~ 90.00
Independent Claims	3 ~~2~~	~~3~~ 2	0	x $84 =	$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					~~$0~~ 90.00

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

20575
PATENT TRADEMARK OFFICE

Joseph S. Makuch
Reg. No. 39,286

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON D.C. 20231
ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON D.C. 20231
ASSISTANT COMMISSIONER FOR TRADEMARKS, 2900 CRYSTAL DRIVE ARLINGTON VA 22202-3513
ON 11-13-02

#7 Amdt a 1/8/03 arj

PATENT APPLICATION
Do. No. 9898-188

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Mun-Mo JEONG

Serial No. 10/003,386 Examiner: Gebremariam, Samuel A

Confirmation No. 5232

Filed: October 30, 2001 Group Art Unit: 2811

For: SEMICONDUCTOR DEVICE WITH CONTACTS HAVING UNIFORM CONTACT RESISTANCE AND METHOD FOR MANUFACTURIG THE SAME

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION

Responsive to the Office Action, dated August 14, 2002, please amend the application as follows.

IN THE CLAIMS

cl sub B27

1. (Once amended) A method for manufacturing a semiconductor device comprising:

forming plural interconnection layers, each including a capping layer, the capping layer defining a contact resistance, and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection layers;

forming first contact holes in the interlayer insulating layer, thereby exposing a surface of the etching stopper;

removing a portion of the etching stopper exposed by the first contact holes, thereby forming second contact holes, to leave the capping layers of the plural interconnection layers at substantially the same thickness such that the contact resistances of the plural interconnection layers are substantially uniform; and

forming a conductive layer within the second contact holes.